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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,086	10/18/1999	WARREN M. FARNWORTH	98-0105.01	2322

7590 10/06/2004

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/420,086	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-39 and 47-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-39 and 47-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10-18-99* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on has been entered. An action on the RCE follows.

2. The amendment filed on 07/12/04 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

4. Claims 25, 35, 47 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568).

Regarding clam 25, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:

- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53, Col. 10, line 29, Col. 16, line 46) having top and bottom surfaces
- a conductive layer comprising a metal alloy/conductive layer of a predetermined/selected thickness (see 512/1011a-1011d in Fig. 10A/10B; Col. 10, lines 30-53) having elements/land segments comprising a plurality of first portions (1011a and 1011d in Fig. 10A/10B) and a plurality of second portions (1011b, 1011c and 512 in Fig. 10A/10B), the metal alloy comprising a conventional material such as copper (Col. 10, line 38, Col. 17, line 32)
- a plurality of conductors on the first and second portions comprising conductive pads/sites (not numerically referenced- see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A), those on the first portions being separated and electrically isolated from one another by those on the second portions of the conductive layer (see 1011a/1011d being spaced from 101 lb in Fig. 10A/10B)
- a plurality of recesses/grooves (not numerically referenced- see recesses/grooves having predetermined size, shape and width in Fig. 10A/10B between the conductive portions of the conductive layer) in the conductive layer defining a size, a spacing and a shape (Col. 11, lines 20-24) of the conductors and the second portions of the conductive layer

- a semiconductor die (die 502 in Fig. 10A/10B) being mounted on the top surface of the substrate in an electrical communication with the conductors comprising conductive portions/conductive pads
- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors/conductive pads (1011a, 101 lb, etc. respectively in Fig. 10A), and
- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conductive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 15).

Chou et al. fail to teach the conductive metal layer substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for electrical transmission and no electrical transmission respectively.

Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the first or

second portions of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65). Such land/pad connections further comprise one or more connections configured for grounded/no electrical transmission separated by those configured for electrical transmission (see Col. 16, line 5- Col. 17, line 50).

Furthermore, determination of parameters such as conductor dimensions including conductor area, thickness, width/spacing, shape/profile, etc., die pad area, pad/via dimensions, number of such conductors/pads/vias, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical characteristics including impedance, signal-to-noise ratio, grounding, etc., operating speed, performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive metal layer substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for electrical transmission and no electrical transmission respectively as taught by the embodiment of Fig. 11A/11B in Chou et al. so that the thermal dissipation and electrical performance/grounding can be improved in Chou et al's component.

Regarding claim 25, forming the elements of the components do not distinguish over Chou et al., because only the final product/structure is relevant, not the process of forming the elements such as "forming elements by deep UV-photo processing/plasma etching", "forming elements by E-beam exposure/reactive ion-etching or sputtering" or "laser machining". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 35, Chou et al. teach substantially the entire claimed structure as applied to claim 25 above.

Regarding claim 47, Chou et al. teach substantially the entire claimed structure as applied to claim 25 above, wherein Chou et al. teach the each conductor having opposing edges (see vertical edges of 1011a-1011d in Fig. 10A) being

defined by a pair of grooves/recesses (see the pair of grooves/recesses on both sides of 1011a-1011d in Fig. 10A) and each conductor having the portions of the conductive layer on either side being separated from the opposing edges by the pair of grooves/recesses.

Regarding claim 51, Chou et al. teach substantially the entire claimed structure as applied to claim 47 above, wherein Chou et al. teach the conductive layer (512/1011a-1011d in Fig. 10A/10B) having an opening in a central portion for attaching/bonding the die to the substrate (see Fig. 10A).

3. Claims 26, 27, 29, 30, 32, 33, 36, 37, 48-50, 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Rostoker et al. (US Pat. 6181011).

Regarding claims 26, 27, 29 and 48-50, Chou et al. teach substantially the entire claimed structure as applied to claims 25 and 47 above, wherein Chou et al. further teach using a reduced pitch between the lands/pads and using shorter bonding wires to provide reduced impedance and improved manufacturing yield and reliability (Col. 16, lines 55-37), but Chou et al. fail to teach each conductor or each groove having a width/first width and a width/second width as small as about 5 microns respectively.

Rostoker et al. disclose prior art (see Liu et al, US Pat. 5693568, Pub. date-Dec. 1997) teaching having conventional semiconductor packages comprising conductor/interconnect pattern having feature size/width and spacing being 0.3-0.4 microns or greater (see Liu et al., Col. 1, line 61) and further discloses Liu et al's devices having conductor width/spacing as low as 0.35 microns or less to improve operating speed and to reduce signal-to-noise ratio (see Liu et al., Col. 3, lines 59-67).

Furthermore, determination of parameters such as conductor dimensions including thickness, area, width/spacing, etc., die pad area, pad/via dimensions, shape/profile, number of such conductors/pads/vias, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical characteristics including impedance, signal-to-noise ratio, etc., operating speed, performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate each conductor or each groove having a width/first width and a width/second width as small as about 5 microns respectively as taught by Rostoker et al. so that the capacitance and interconnect delay can be reduced, the desired impedance value can be achieved and the speed/performance of the package can be improved in Chou et al's component.

Regarding claim 30, Chou et al. and Rostoker et al. teach substantially the entire claimed structure as applied to claims 25-27 above.

Regarding claim 32, Chou et al. and Rostoker et al. teach substantially the entire claimed structure as applied to claim 30, wherein Chou et al. teach the plurality of conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the respective conductors (1011a, 1011b, etc. respectively in Fig. 10A) and the plurality of external contacts/contact balls (not numerically referenced in Fig. 10A- see 522 a-522e in Fig. 5B; Col.16, lines 46-53) on the bottom/second surface of the substrate.

Regarding claim 33, Chou et al. and Rostoker et al. teach substantially the entire claimed structure as applied to claim 30, wherein Chou et al. teach the component comprising the assembly/package (1000 in Fig. 10A/10B; Col. 16, line 39).

Regarding claims 36 and 37, Chou et al. and Rostoker et al. teach substantially the entire claimed structure as applied to claims 35 and 25-27 above.

Regarding claims 52 and 53, Chou et al. and Rostoker et al. teach substantially the entire claimed structure as applied to claims 25-27 and 29 above.

4. Claims 28, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Rowe et al. (US Pat. 4739448).

Regarding claims 28, 38 and 39, Chou et al. teach substantially the entire claimed structure as applied to claims 25 and 35 respectively above, except the selected thickness of the metal being about 18 microns.

Rowe et al. teach a package having a semiconductor component on a substrate where a conductive metal layer on the substrate has a thickness about 1 mil or 25 microns (see 26 in Fig. 3; Col. 3, line 64, Col. 9, line 12).

Furthermore, determination of parameters such as conductor thickness, width/spacing, pad/via dimensions, shape/profile, number of such conductors/pads/vias, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical characteristics including impedance, signal-to-noise ratio, etc., operating speed, performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the thickness of the metal being about 18 microns as taught by Rowe et al. so that the desired electrical characteristics can be achieved and metallization/patterning can be optimized in Chou et al's component.

5. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) and Rostoker et al. (US Pat. 6181011) as applied to claim 30 above, and further in view of Rowe et al. (US Pat. 4739448).

Regarding claim 31, Chou et al., Rostoker et al. and Rowe et al. teach substantially the entire claimed structure as applied to claims 30, 25 and 28 above.

6. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) and Rostoker et al. (US Pat. 6181011) as applied to claim 30 above, and further in view of Pedder (US Pat. 5717245).

Regarding claim 34, Chou et al. and Rostoker et al. teach substantially the entire claimed structure as applied to claim 30, except an encapsulant at least partially covering the die and a portion of the surface.

Pedder teaches using a sealant/encapsulant to encapsulate the BGA package/module (Col. 1, line 55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the encapsulant covering the die and a portion of the surface as taught by Pedder so that the surface protection for the electrical connections can be improved and the damage from contamination and moisture can be reduced in Rostoker et al. and Chou et al's component.

Response to Arguments

7. Applicant's arguments filed on 07-12-04 have been fully considered but they are not persuasive.

A. Applicant contends that Rostoker et al's reference has the effective date of Dec. 1998, which is after the priority date (July 1998) of the invention.

However, Rostoker et al. disclose the prior art reference by Liu et al. having the publication date of Dec. 1997.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

NITIN PAREKH

10-01-04

PATENT EXAMINER

TECHNOLOGY CENTER 2800